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10/626,124	07/23/2003	Hiroharu Sakai	16869P-079300US	9522

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EXAMINER	
PATEL, GAUTAM	

ART UNIT	PAPER NUMBER
2627	

DATE MAILED: 06/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/626,124	SAKAI ET AL.	
	Examiner	Art Unit	
	Gautam R. Patel	2627	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6-21* is/are rejected.

7)☒ Claim(s) *5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-21 are pending for the examination.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. § 119(a)-(d), which papers have been placed of record in the file.

Drawings/Objection

3. The drawings are objected for following reasons:

The drawings are objected to under 37 C.F.R. § 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, "a reproduction system circuit, a speed information detection circuit, a position detection unit, an accessing unit and a setting unit" must be shown or the features cancelled from the claims.

No new matter should be entered.

Applicant is required to submit a proposed drawing correction in response to this Office Action. Any proposal by the applicant for amendment of the drawings to cure defects must consist of following:

Drawing changes must be made by presenting replacement figures which incorporate the desired changes and which comply with 37 CFR 1.84. An explanation of the changes made must be presented either in the drawing amendments, or remarks, section of the amendment, and may be ***accompanied by a marked-up copy of one or more of the figures being amended, with annotations***. Any replacement drawing sheet ***must be identified in the top margin as "Replacement Sheet"*** and include all of the figures appearing on the immediate prior version of the sheet, even though only one figure may be amended. ***Any marked-up (annotated) copy showing changes must be labeled "Annotated Marked-up Drawings" and accompany the replacement sheet in the amendment (e.g., as an appendix).***

a proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance. Correction may not be held in abeyance.

Correction are required.

Specification

4. The disclosure is objected for following reasons.

The title of the invention is neither precise nor descriptive. A new title is required which should include, using twenty words or fewer, claimed features that differentiate the invention

from the Prior Art. It is recommended that the title should reflect the gist of or the improvement of the present invention.

Correction is required.

Claim Rejections - 35 U.S.C. § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 9-21are rejected under 35 U.S.C. § 102(e) as being anticipated by Masuda et al., US. patent Application 2004/0066722 (hereafter Masuda).

As to claim 1, Masuda discloses the invention as claimed, an optical disk apparatus [see Figs. 2-3] including an optical pickup, an optical disk, a reproduction system circuit, a speed information detection circuit, a position detection unit, an accessing unit and a setting unit configured, comprising:

an optical pickup [fig. 2, unit 4] configured to irradiate an optical disk [fig. 2, unit 100] with a beam, to receive light reflected from the optical disk, and to convert the reflected light into an electrical signal [paragraphs 19];

a processor [fig. 2, units 10-15] including: a reproduction system circuit [fig. 2, units 14, 11 & 3] configured to generate a reproduction signal used in restarting recording of the optical disk after an interruption, based on the electrical signal from the optical pickup and setting values [paragraphs 25-30];

a speed information detection circuit [fig. 2, unit 11] configured to detect speed information before or after an interruption of a recording on the optical disk based on the electrical signal from the optical pickup [paragraph 35]; and

a position detection unit [fig. 2, unit 11] configured to detect a recording restart position and a current position of the optical disk;

an accessing unit [fig. 2, unit 11] configured to control the optical pickup to access the optical disk at the recording restart position from the current position of the optical disk; and

a setting unit configured [fig. 2, unit 11] to set in the reproduction system circuit setting values based on the detected speed information, the setting values being used by the reproduction system circuit to generate the reproduction signal [paragraphs 63-77].

6. The aforementioned claim 2, recites the following elements, inter alia, disclosed in Masuda:

a recording restart speed for restarting recording is the detected speed from the speed information detection circuit [paragraphs 7, 11 & 35].

7. The aforementioned claim 3, recites the following elements, inter alia, disclosed in Masuda:

the recording restart position on the optical disk is the position on which recording occurred before the interruption at an interrupted position on the optical disk [paragraphs 7, 11 & 35].

8. The aforementioned claim 9, recites the following elements, inter alia, disclosed in Masuda:

a memory [fig. 2, units 27-28] for storing recording speed information sent from the speed information detection circuit, wherein, if there is a recording interruption request, speed information before the recording interruption request, which is stored in the memory, is read out [paragraphs 33-34 and 44]

9. The aforementioned claim 10, recites the following elements, inter alia, disclosed in Masuda:

a memory for storing recording speed information sent from the speed information detection circuit, wherein, if there is a recording interruption request, speed information of a sector which is a predetermined number of sectors short of the recording interruption request is read out from the memory [paragraphs 33-34 and 44].

10. The aforementioned claim 11, recites the following elements, inter alia, disclosed in Masuda:

the speed information detection circuit detects speed information during a period ranging from after a recording interruption request to when the optical pickup starts accessing the sector before the interrupted position [paragraphs 63-77].

11. The aforementioned claim 12, recites the following elements, inter alia, disclosed in Masuda:

the speed information detection circuit detects speed information after the optical pickup accesses to and lands on the sector before the interrupted position subsequent to a recording interruption request [paragraphs 63-77].

12. The aforementioned claim 13, recites the following elements, inter alia, disclosed in Masuda:

the speed information detection circuit comprises a wobble detection circuit configured to extract a wobble signal, and a wobble cycle detection circuit configured to measure a carrier frequency of the wobble signal detected by the wobble detection circuit and detect speed information before or after an interruption of the recording on the optical disk; and wherein the position detection unit comprises an ATIP detection circuit configured to detect a current position which is used for accessing a sector before a position of the recording interruption after a recording interruption from ATIP address information indicating absolute time information of the disk based on the wobble signal obtained from the wobble detection circuit [paragraphs 63-77].

13. The aforementioned claim 14, recites the following elements, inter alia, disclosed in Masuda:

a memory for storing recording speed information obtained by one of the wobble cycle detection circuit and the ATIP cycle detection circuit, wherein, if there is a recording interruption request, speed information before the recording interruption request, which is stored in the memory, is read out [paragraphs 33-34 and 44]

14. The aforementioned claim 15, recites the following elements, inter alia, disclosed in Masuda:

the speed information detection circuit comprises a wobble signal detection circuit configured to detect a wobble signal, and an ATIP cycle detection circuit configured to detect a cycle at which ATIP address information is obtained from the detected wobble signal to detect speed information before or after an interruption of the recording on the optical disk; and wherein the position detection unit comprises an ATIP detection circuit configured to detect a current position which is used for accessing a sector before a position of a recording interruption after the recording interruption from ATIP address information indicating absolute time information of the disk based on the wobble signal obtained from the wobble detection circuit [paragraphs 63-77].

15. As to claim 16, it is rejected for the similar reasons set forth in the rejection of claim 1, supra. As to the added limitations of a recording synchronization clock and clock cycle detector, Masuda discloses this in figure 2, units 20, 21 and 13.

16. As to claim 17, it is drawn to a method corresponding to the apparatus of claim 1, and is therefore rejected for similar reasons set forth in the rejection of claim 1, above.

17. The aforementioned claim 18, recites the following elements, inter alia, disclosed in Masuda:

detecting the recording speed includes a step of reading out speed information before the recording interruption request [paragraphs 63-77].

18. The aforementioned claim 19, recites the following elements, inter alia, disclosed in Masuda:

detecting the recording speed includes a step of reading out speed information of a sector which is a predetermined number of sectors short of the recording interrupted request [paragraphs 63-77].

19. The aforementioned claim 20, recites the following elements, inter alia, disclosed in Masuda:

detecting the recording speed includes a step of reading out speed information during a period ranging from after the recording interruption request to when the optical pickup starts accessing the sector before the interrupted position [paragraphs 63-77].

20. The aforementioned claim 21, recites the following elements, inter alia, disclosed in Masuda:

detecting the recording speed includes a step of reading out speed information after the optical pickup accesses to and lands on the sector before the interrupted position subsequent to the recording interruption request [paragraphs 63-77].

Claim Rejections - 35 U.S.C. § 103

21. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 4 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Masuda as applied to claims 1-3 above in view of Ata et al., US. patent 5,027,338 (hereafter Ata).

As to claim 4, Masuda discloses all of the above elements, including an equalizer circuit configured to extract an information signal of the optical disk from the electrical signal sent from the optical pickup so as to perform a waveform equalization and a group delay smoothing of an EFM signal [fig. 1, units 12-14; paragraphs 23-25]. Masuda does not specifically discloses an HPF circuit to suppress fluctuations of voltage level when a scratch passes or a binarization circuit and scratch zone detection circuit.

However, HPF [for signal smoothing] and scratch detections are well known in the art for a while, Also more importantly Ata clearly discloses:

an HPF circuit [fig. 2, unit F_H] configured to suppress a fluctuation in binary voltage level of the EFM signal when a scratch passes; a binarization circuit [fig. 2, unit I] configured to binarize the signal sent from the HPF circuit ;

a PLL circuit configured [fig. 2, unit I] to generate a synchronizing clock from the binarized signal; a demodulation circuit configured to convert information written on the optical disk into a digital data string by using the binarized signal and the synchronizing clock; and

a scratch zone detection circuit [fig. 2, unit A_7 & SW_3] configured to generate scratch zone information by using the information signal of the optical disk obtained by the optical pickup [col. 2, line 47 to col. 3, line 54].

Both Masuda and Ata are interested in improving the tracking mechanism in an optical disk device.

One of ordinary skill in the art at the time of invention would have realized that the circuit of Masuda would susceptible to high voltage spikes due defects such as scratch etc., which are normally found on a disc that would have compromised the quality of the electrical signals.

Therefore, it would have been obvious to have used a HPF circuit in the system of Masuda as taught by Ata because one would be motivated to reduce noise in the system of Masuda due to scratch and provide better signal controls and improve quality of the signal by providing smoother voltage & current waveforms thus avoid driving actuator on the basis of the different error signal and swing to a abnormally large value [col. 3, lines 45-54; Ata].

22. Claims 6-8 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Masuda as applied to claims 1-3 above, and further in view of Wang et al., US. patent application 2004/0017745 [hereafter Wang].

As to claim 6, Masuda discloses all of the above elements, including PLL circuit configured to generate a synchronized clock [paragraphs 60] & the speed information detection circuit comprises a wobble signal detection circuit configured to detect a wobble signal as explained above. Masuda does not specifically discloses well known details of the PLL and circuits associated with it or that the carrier frequency is extracted by the PLL.

However, PLL and associated details are well known in the art for a while, Also more importantly Wang clearly discloses:

a wobble cycle measurement circuit configured to measure a carrier frequency of the detected wobble signal [paragraph 13].

Both Masuda and Wang are interested in improving the tracking mechanism in an optical disk device and generating ATIP signals and wobble signals. Both show CLV and CAV type speed control.

One of ordinary skill in the art at the time of invention would have realized that keeping speed at constant rotation speed would increase the efficiency of the system and it is a good characteristic to have.

Therefore, it would have been obvious to have used a PLL circuit with associated details such as measuring carrier frequency in the system of Masuda as taught by Wang because one would be motivated to keep spindle at constant speed and avoid increasing or decreasing the speed according to rotation radius, thus reducing the precision control that is otherwise needed, thus saving money and components in the system [paragraph 9; Wang].

23. The aforementioned claim 7, recites the following elements, inter alia, disclosed in Wang:

the speed information detection circuit comprises a wobble signal detection circuit configured to detect a wobble signal and an ATIP cycle detection circuit configured to detect from the detected wobble signal a cycle from which ATIP address information is obtained [paragraphs 13-17].

24. The aforementioned claim 8, recites the following elements, inter alia, disclosed in Wang:

the speed information detection circuit comprises a recording synchronizing clock generation circuit configured to generate a recording synchronizing clock in response to a recording speed, and a clock cycle detection circuit configured to detect a cycle of the recording synchronizing clock generated by the recording synchronizing clock generation circuit [paragraphs 13-17].

Allowable Subject Matter

25. Claim 5 is objected as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

NOTE: Claim 5 is allowable over the prior art of record since the cited references taken individually or in combination fails to particularly disclose a disk apparatus which includes optical head & processor which includes an equalizer and a setting value circuit wherein " one of the frequency characteristics of the equalizer circuit and the HPF circuit, response characteristic of the binarization circuit, gains of PLL circuit and servo circuit and a time constant of the scratch zone detection circuit".

It is noted that the closest prior art, Ata (US 5,027,338) shows a similar apparatus which has almost all the elements including a time constant [fig. 2, t_3] . However Ata fails to disclose all of the above components that are generating this signal.

Other prior art cited

26. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Iida et al. (US. Patent application 2002/0021637 A1).
b) Heemskerk et al. (US. Patent application 2005/0068874 A1).
c) Hayashi (US. patent 6/594,213).
d) Abe et al. (US. patent 6,801,489)

Contact information

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gautam R. Patel whose telephone number is 571-272-7625. The examiner can normally be reached on Monday through Thursday from 7:30 to 6.

The appropriate fax number for the organization (Group 2650) where this application or proceeding is assigned is 571-273-8300.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Dwayne Bost, who can be reached on (571) 272-7023.

Any inquiry of a general nature or relating to the status of this application should be directed to the Electronic Business Center whose telephone number is 866-217-9197 or the USPTO contact Center telephone number is (800) PTO-9199.

GAUTAM R. PATEL
PRIMARY EXAMINER

Gautam R. Patel
Primary Examiner
Group Art Unit 2627

June 27, 2006